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10/817,392	04/02/2004	Wayne D. Young	019680-009100US	2905

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EXAMINER	
TRAN, TRANG U	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/817,392	YOUNG ET AL.	
	Examiner	Art Unit	
	Trang U. Tran	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 3/27/07 have been fully considered but they are not persuasive.

In re pages 7-8, applicants argue, with respect to claims 1-10 and 17-19, that Rinaldi does not teach or suggest "an encoder coupled to an output of the pixel pipeline circuit and configured to convert the pixel stream to digital sample values for a target analog signal representing the pixel stream in the target format, thereby generating a base data stream at a base sampling rate" and "a supersampling circuit coupled to an output of the encoder and configured to generate a supersampled data stream at a supersampling rate from the base data stream, the supersampling rate being higher that the base sampling rate".

In response, the examiner respectfully disagreed. Rinaldi et al discloses in col. 3, lines 35-47 that "FIG. 2 illustrates a schematic block diagram of the video decoder 20, the output control module 21 and the DAC module 23. The video decode 20 includes a multiplexor 50, an analog digital conversion module 54, a comb filter 52, and a YCrCb processing module 56. Te analog-to-digital conversion module 54 includes two analog-to-digital conversion module 54 includes two analog-to-digital converters 58 and 60 and two decimation filters 62 and 64. The multiplexor 50 is operably coupled to receive the video input signals 28 and, based on a select signal, provides the selected video signals to the analog-to-digital conversion module 54. The A/D conversion module 54 receives the analog signals, converts them to digital signals, and then filters them to produce

digital video signals 78". From the above passage, it is clear that the analog-to-digital conversion module 54 converts the pixel stream to digital sample values for a target analog signal representing the pixel stream in the target format and generates a base data stream at a base sampling rate. Thus the claimed "an encoder" is anticipated by the A/D conversion module 54 of Rinaldi et al. Rinaldi et al additionally discloses in col. 3, lines 57-59 that "The output control module 21 includes a YCrCb to YUV converter 66, the input switching matrix 68, up sample module 70, and an output switching matrix 72". It is noted that the up sample module 70 of Rinaldi et al would upsamples the digital signal with higher sampling rate. Thus, the claimed "a supersampling circuit" is anticipated by the up-sampling module 70 of Rinaldi et al. It is noted that the video signal of Rinaldi et al is displayed on the display screen and; therefore, the video signal of Rinaldi is pixel stream as required by claims.

In re pages 8-9, applicants argue, with respect to claims 11-16 and 20-22, that Rinaldi does not teach or suggest "a supersampling circuit coupled to an output of the pixel pipeline circuit and configured to generate a supersampled pixel stream comprising a second number of digital pixel values per line, the second number being greater than the first number, at a supersampling rate higher than the base pixel rate" and "an encoder coupled to an output of the supersampling circuit and configured to convert the supersampled pixel stream to digital sample values for a target analog signal representing the supersampled pixel stream in the target format, thereby generating a supersampled data stream at an enhanced sampling rate".

In response, the examiner respectfully disagreed. As discussed above, the claimed "a supersampling circuit" is anticipated by the up sample module 70 of Rinaldi et al. Rinaldi et al discloses in col. 4, lines 8-16 that "The output switching matrix 72, which may include a plurality of multiplexors, receives the output of the up sampling module 70 and the YUV video data 80 from the video encoder 22. Based on output commands, the output switching matrix 72 provides the output of the up sampling module 70, the YUV video data 80, or a combination thereof to the digital-to-analog conversion module 23. As shown, the DAC module 23 includes three separate digital-to-analog converters". From the above passage, it is clear the output switching matrix 72 converts the supersampled pixel stream to digital sample values for a target analog signal representing the supersampled pixel stream in the target format and generates a supersampled data stream at an enhanced sampling rate. Thus, the claimed "an encoder" is anticipated by the output switching matrix 72 of Rinaldi et al.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 5-8, 11-12 and 15-22 are rejected under 35 U.S.C. 102(b) as being anticipate by Rinaldi et al (US Patent No. 6,327,002 B1).

In considering claim 1, Rinaldi et al discloses all the claimed subject matter, note 1) the claimed a pixel pipeline circuit configured to provide a pixel stream comprising

digital pixel values is met by the multiplexer 50 and the ADCs 58, 60 (Fig. 2, col. 2, lines 51-67 and col. 3, lines 36-48), 2) the claimed an encoder coupled to an output of the pixel pipeline circuit and configured to convert the pixel stream to digital sample values for a target analog signal representing the pixel stream in the target format, thereby generating a base data stream at a base sampling rate is met by the input switching matrix 68 (Fig. 2, col. 3, line 45 to col. 4, line 7), 3) the claimed a supersampling circuit coupled to an output of the encoder and configured to generate a supersampled data stream at a supersampling rate from the base data stream, the supersampling rate being higher than the base sampling rate is met by the up sampling module 70 which changes the sampling frequency of the signals to match the desired output sampling frequencies (Fig. 2, col. 3, line 45 to col. 4, line 7), and 4) the claimed a digital to analog converter coupled to an output of the supersampling circuit and configured to convert the supersampled data stream to an analog output signal is met by the DAC module 23 (Fig. 2, col. 4, lines 8-16).

In considering claim 2, the claimed wherein the supersampling rate is selected so as to provide substantial attenuation of a higher frequency echo in the analog output signal, the higher frequency echo occurring in a frequency band above a baseband of the analog output signal is met by the up sampling module 70 which changes the sampling frequency of the signals to match the desired output sampling frequencies (the rate is selected from the input switching matrix 68) (Fig. 2, col. 3, line 45 to col. 4, line 7).

In considering claim 5, the claimed wherein the baseband of the analog output signal is determined with reference to a baseband for a standard definition television monitor is met by the processing the incoming video signal through plurality of output video sources (Fig. 4, col. 4, line 44 to col. 6, line 20).

In considering claim 6, the claimed wherein the baseband of the analog output signal is determined with reference to a baseband for a high definition television monitor is met by the processing the incoming video signal through plurality of output video sources (Fig. 4, col. 4, line 44 to col. 6, line 20).

In considering claim 7, the claimed wherein the encoder is further configured to respond to one or more control parameters, thereby enabling selection of one of a plurality of candidate formats as the target format is met by the input switching matrix 68 (Fig. 2, col. 3, line 45 to col. 4, line 7).

In considering claim 8, the claimed wherein the plurality of candidate formats includes a standard definition television format and a high definition television format is met by input switching matrix 68 which provides the YUV data provided by the YcrCb to YUV converter 66, or selects the Y and C component digital signals 74, 76 or combination of the Y and C component digital signals and the YUV signals to the up sampling module 70 (Fig. 2, col. 3, line 45 to col. 4, line 7).

In considering claim 11, Rinaldi et al. discloses all the claimed subject matter, note 1) the claimed a pixel pipeline circuit configured to provide a pixel stream comprising a first number of digital pixel values per line at a base pixel rate is met by the multiplexer 50 and the ADCs 58, 60 (Fig. 2, col. 2, lines 51-67 and col. 3, lines 36-48),

2) the claimed a supersampling circuit coupled to an output of the pixel pipeline circuit and configured to generate a supersampled pixel stream comprising a second number of digital pixel values per line, the second number being greater than the first number, at a supersampling rate higher than the base pixel rate is met by the up sampling module 70 which changes the sampling frequency of the signals to match the desired output sampling frequencies (Fig. 2, col. 3, line 45 to col. 4, line 7), 3) the claimed an encoder coupled to an output of the supersampling circuit and configured to convert the supersampled pixel stream to digital sample values for a target analog signal representing the supersampled pixel stream in the target format, thereby generating a supersampled data stream at an enhanced sampling rate is met by the output switching matrix 72 (Fig. 2, col. 3, line 57 to col. 4, line 16), and 4) the claimed a digital to analog converter coupled to an output of the encoder and configured to convert the supersampled data stream to an analog output signal is met by the DAC module 23 (Fig. 2, col. 4, lines 8-16).

Claim 12 is rejected for the same reason as discussed in claim 2.

Claims 15-16 are rejected for the same reason as discussed in claims 7-8, respectively.

Claim 17 is rejected for the same reason as discussed in claims 1-2 and further the claimed a pixel generator circuit configured to generate and store pixel data for a frame of an image is met by the multiplexer 50 and the ADCs 58, 60 (Fig. 2, col. 2, lines 51-67 and col. 3, lines 36-48).

Claims 18-19 are rejected for the same reason as discussed in claims 7-8, respectively.

Claim 20 is rejected for the same reason as discussed in claims 1 and 2.

Claims 21-22 are rejected for the same reason as discussed in claims 7-8, respectively.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rinaldi et al (US Patent No. 6,327,002 B1).

In considering claim 9, Rinaldi et al disclose all the limitations of the instant invention as discussed in claim 1 above, except for providing the claimed wherein the supersampling rate is substantially equal to twice the base sampling rate. The capability of using the supersampling rate is substantially equal to twice the base sampling rate is old and well known in the art. Therefore, the Official Notice is taken. It would have been obvious to one ordinary skill in the art at the time of the invention to incorporate the old and well known using of the supersampling rate is substantially equal to twice the base sampling rate into Rinaldi et al's system in order to increase the quality of the video signal during sampling process.

In considering claim 10, Rinaldi et al disclose all the limitations of the instant invention as discussed in claim 1 above, except for providing the claimed wherein the supersampling rate is substantially equal to four times the base sampling rate. The capability of using the supersampling rate is substantially equal to four times the base sampling rate is old and well known in the art. Therefore, the Official Notice is taken. It would have been obvious to one ordinary skill in the art at the time of the invention to incorporate the old and well known using of the supersampling rate is substantially equal to four times the base sampling rate into Rinaldi et al's system in order to increase the quality of the video signal during sampling process.

6. Claims 3-4 and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rinaldi et al (US Patent No. 6,327,002 B1) in view of the admitted prior art (Fig. 1A, 1B, page 2, [0005]-[0006]).

In considering claim 3, Rinaldi et al disclose all the limitations of the instant invention as discussed in claim 1 above, except for providing the claimed further comprising an electromagnetic interference (EMI) filter coupled to an output of the digital to analog converter and configured to substantially attenuate frequency components of the analog output signal above a maximum frequency. The admitted prior art teaches that the monitor path 120 includes a pixel pipeline 122, an encoder 124, a DAC 126, and an electromagnetic interference (EMI) filter 128, which is simply a low pass filter with a frequency cut off above about 200 MHz (Fig. 1A, 1B, page 2, [0005]-[0006]). Therefore, it would have been obvious to one ordinary skill in the art at the time of the invention to incorporate the EMI filter as taught by the admitted prior art

into Rinaldi et al's system in order to limit the high frequency radiation emitted by electronic devices.

In considering claim 4, the claimed wherein the supersampling rate is selected so as to substantially attenuate an echo of the analog output signal, the echo appearing in a frequency band between a baseband of the analog signal and the maximum frequency is met by the up sampling module 70 which changes the sampling frequency of the signals to match the desired output sampling frequencies (the rate is selected from the input switching matrix 68) (Fig. 2, col. 3, line 45 to col. 4, line 7 of Rinaldi et al).

Claim 13 is rejected for the same reason as discussed in claim 3.

Claim 14 is rejected for the same reason as discussed in claim 4.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trang U. Tran whose telephone number is (571) 272-7358. The examiner can normally be reached on 8:00 AM - 5:30 PM, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TRANG U. TRAN
PRIMARY PATENT EXAMINER

June 10, 2007

Trang U. Tran
Primary Examiner
Art Unit 2622